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10/088,028	03/14/2002	Shinji Furusho	KUBOTA 0007	6569

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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/088,028	FURUSHO, SHINJI	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-13 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-13 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 12 and 13 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for claim 1-11, does not reasonably provide enablement for limitation of the plurality of sets of buses are connected in parallel to the CPU and to each memory module. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to connect the plurality of sets of buses in parallel to the CPU and the each memory module the invention commensurate in scope with these claims. Note a parallel connection is a " connection of two or more parts of a circuit to the same pair of terminals" (Definintion form Dictionary of Computers Information processing and telecommunication 2nd Ed by Jerry M Rosemberg copyright 1987 on page 451. The figure 1 in the instant application shows that the CPU and memory modules are connected to a plurality of buses. The buses are depicted as oriented parallel to each other however the connection to the CPU provides only one input and one output so the CPU can only connect to one bus for input at a time and one bus for output at a time. Also the connection does not provide for simultaneous transmission of data to/from a plurality of memory module in the same direction (input or output) via any one set or buses. The connections provide for a system where an arbitration for

control of each of the buses for transmission via a selected bus. Therefore in operation the system would require the CPU or memory module to gain exclusive access to a particular set of buses so data could be transmitted. The bus used would have had to have its connection to the other memory modules disconnected (e.g., tristated) So in operation the sets of buses are connected in a shared manner and not in parallel to each of the memory modules and CPU. If indeed they were connected in parallel to each of the sets of buses then no arbitration would be necessary because each module or CPU could simultaneously send data to/from each other memory module or CPU without arbitrating for access to the bus. The System allows for connection each module to transmit via a separate bus however since the CPU only has one input an output the CPU as disclosed cannot operate in this manner. Therefore parallel connection of the buses to the CPU and each memory module cannot be achieved as disclosed. In addition assuming a memory module could send data to another memory module as disclosed this would entail the CPU and one memory module transmitting on one bus while the other two memory module are connected to a shared connection for transmitting data therebetween. Also there is no indication that the CPU or any of memory modules can each send and received data on different buses at the same time which would be required for the simultaneous connections.

3. This rejections are of claims 1-11 are maintained as set forth in the last office action and repeated below.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 6 recites the limitation "said bus and memory module in claim 6. There is insufficient antecedent basis for this limitation in the claim. Multiple buses and memory modules have been defined and it is unclear as to which is being referred. The Examiner is taking the claim to mean " a bus and a memory module:" since there are so many of each defined in an effort to fit the context and give the broadest reasonable interpretation.

6. This rejection is maintained as set forth in the last office action and repeated above.

Claim Rejections - 35 USC § 103

7. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thiel (EP 0408 810 A1) in view of Hennessy (Computer Organization and Design).

In regard to claim 1,

a. Thiel discloses a parallel computer (figure 5) comprising:

i. a CPU module (figure 5, element 56, a plurality of memory modules (figure 5, elements 32a-32p), each of which having a processor (figure 5, element 48a) and memory core (figure 5, element 50a), and a plurality of sets of buses that make connections between said CPU and memory modules and/or connections among memory modules (figure 5 shows various buses connecting the memory modules (Processors a-p) to each other and to the CPU (control processor), wherein the processors

or the various memory modules operate on an instruction given by the CPU to the processors of the various memory, [Column 2, lines 39-42 show that the parallel computer system executes instructions. Column 4, lines 4-6 and figure 5 show that the control processor (CPU) supplies control data (instructions) to the control bus 54 for control of the modules in the system.]

ii. and wherein said architecture of a parallel computer is constituted such that: a series of data having a stipulated relationship is given a space ID such that: a series of data having a stipulated relationship is given a space ID and the processor of each module manages a table that contains at least said space ID, the logical address of the portion of the series of data that it manages itself, the size of said portion and the size of the series of data,[See column 3, line 4-column 4, line1 and figure 8, where the MD Decoder and Address Generator of figure 5 that is within each memory module is illustrated. It is shown that data (having a relationship of being used by the processor) is uniquely labeled (a space ID) for identification and that the processor in each module detects the data and thus the ID is inherently stored so there is something to compare when detecting. It is also shown that an address of data is decoded and translated for access to main memory and thus stored for use. In addition figure 8 shows several registers (e.g., 140, 142, 112, 114, 118, 120, and 134) that store

addresses of data of which the processor in the memory module manages. Also shown in that figure and in the text cited above, there are stored upper and lower limits of the addresses and thus a size of the data is known and stored. Since the processor manages all the data it uses, the portion of the series of data is in fact the entire series of data. Further all the collective storage elements that store this data within the processor or memory module are viewed as a table.1]

iii. and the processor of each memory module determines if the portion of the series of data that is manages itself is involved in a received instruction, reads data stored in the RAM core and sends it out on a bus, writes data given via the bus to the RAM core, performs the necessary processing on the data , and/or updates said table. [The Examiner notes that the claim language of this limitation (specifically the placement of the and/or phrase: requires the reference need only show that portion of data managed by the processor performs any of the subsequent functions. As shown in the section cited above, the processor detects if the data is involved in a read or write and sending the data on the bus.]

b. Thiel does not explicitly disclose the memory modules having a RAM core, but only a local memory.

c. Hennessy has disclosed on pages 16 and 18 the use of RAM memory and that RAM (random access memory) differentiates from a

sequential access memory in that memory access take the same amount of time no matter what portion of memory is read.

d. Hennessy has then shown on page 541 that RAM (SRAM and DRAM) have a much faster typical access time than a sequential memory such as a magnetic disk. This quick access time would have motivated one of ordinary skill in the art at the time of invention to modify the design of Thiel to use a RAM as the local memory core rather than a sequential access memory.

8. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Thiel to use RAM as the local memory core rather than a sequential access memory so that typical memory accesses faster.

9. In regard to claim 2, Thiel in view of Hennessy discloses a computer architecture according to claim 1 wherein said processor has:

a. a space comparator that compares the space ID given by the CPU against the space ID of one or more series of data that it manages itself, [As shown above the processor compares the data ID to detect it.]

b. an address comparator that compares the logical address given by the CPU against the logical address of the portion of the data that is manages itself, [As shown in the sections cited above, the address compared with upper and lower limits and thus a comparator exists.]

c. and an address calculator the physical address in its own RAM cell based on said logical address. [Figure 8 shows that the memory address generator is separate from the other circuitry and thus has its own RAM cell.]

10. In regard to claim 3,

a. Thiel in view of Hennessy discloses the computer architecture according to claim 1,

b. Thiel does not explicitly disclose wherein each of said memory modules receives a synchronization signal for achieving synchronization with the CPU module and other memory modules and it is constituted such that it comprises input that is connectable to any of said plurality of sets of buses, and output that is connectable to any of said plurality of buses and at least, it is able to output data according to said synchronization signal by connecting the input to one of said buses, inputting data and connecting the output to any of said buses.

c. Hennessy has taught on page 713 synchronizing multiple processors that share data from a shared memory (such as the memory modules or processors of figure 5 in Thiel, all of which share bulk or main memory 44). This is done with some sort of synchronization signal such as a lock over a bus that connects each processor.

d. Hennessy has taught on this same page that synchronization disallows other processors to work on data before another is finished and thus data integrity and correct results are maintained. The integrity would have motivated one of ordinary skill in the art at the time of invention to modify the design of Thiel in view Hennessy to use synchronization for the multiple processors or memory modules as further taught by Hennessy.

11. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Thiel in view of Hennessy to use synchronization of multiple processors or memory modules as further taught by Hennessy so that data integrity is realized.

12. In regard to claim 4, Thiel in view Hennessy discloses the computer architecture according to claim 3, wherein switches are provided on each of said sets of buses, thereby controlling the connections between said CPU module and the input or output of any of the memory modules, and/or between input and output of one memory module and the output and input of another memory module, and by switching said switches, the exchange of parallel data is achieved in each of said sets of buses. [Column 10, lines 47-50 show that processors (memory modules are switched out when dormant or faulty and thus switches exist in the buses to control which processors receive data in parallel.

13. In regard to claim 5, Thiel in view of Hennessy discloses the computer architecture according to claim 4, wherein the output of one memory module is connected to the output of another memory module via a first bus which is one of said plurality of sets of buses, and the output of said memory module is connected to the input of still another memory module via a second bus which is another one of said plurality of sets of buses, so that the exchange of data over the first bus proceeds in parallel of sets of buses, so that the exchange of data over the first bus proceeds in parallel with the exchange of data over the second bus. [Column 9, line 55-col. 10, line 11 show that data is passed to the data bus from each processor and then written to the destination processor and thus the

input of a second processor is the output of a first and the input of a third processor is the output of the second. The section futher submits that this may be all done in a single pass or in parallel and thus the function is the same the claimed function and thus data bus of Thiel in view of Hennessy must be subdivided into smaller buses via switching to accomplish such.]

14. In regard to claim 6, Thiel in view of Hennessy discloses the computer architecture according to claim 5 wherein the connections between a bus and a memory module are repeated to form multi-stage connections among memory modules. [As shown in figure 5, the connection between the data bus and memory module (processor) 32a is repeated among each module and forms multi-stage (or multi-module where each module is a stage of sorts) connections among memory modules.]

15. In regard to claim 7, Thiel in view of Hennessy the computer architecture according to claim 1, wherein, said processor achieves an instruction to delete an specific element within a series of data, insert a specific element into a series of data, or add a specific element to the end of a series of data, said processor performs a table lookup, compares the region of data that it manages itself against the position of said element subject to deletion, insertion or addition, and based on the results of said comparison, updates the content of said table. [As shown above and in column 3, data is detected by the processor against stored unique labels or ID's for reading data in (insert or addition). This detection is inherently done with a comparator as cited above and the label is stored for future for future write commands to the bus.]

16. In regard to claim 8, Thiel in view of Hennessy discloses the computer architecture according to claim 1, wherein, in response to a given instruction, said processor converts subscripts for specifying elements within a series of data and/or executes value conversion for giving a specific modification to elements. [As shown above, the memory module or processor is responsive to instructions. Column 3 further shows how address values or elements are converted to a linear address.]

17. In regard to claim 9, Thiel discloses a information processing

a. Thiel discloses a parallel computer (figure 5) comprising:

i. a CPU module (figure 5, element 56, a plurality of memory modules (figure 5, elements 32a-32p), each of which having a processor (figure 5, element 48a) and memory core (figure 5, element 50a), and a plurality of sets of buses that make connections between said CPU and memory modules and/or connections among memory modules (figure 5 shows various buses connecting the memory modules (Processors a-p) to each other and to the CPU (control processor), wherein the processors or the various memory modules operate on an instruction given by the CPU to the processors of the various memory, [Column 2, lines 39-42 show that the parallel computer system executes instructions. Column 4, lines 4-6 and figure 5 show that the control processor (CPU) supplies control data (instructions) to the control bus 54 for control of the modules in the system.]

ii. and wherein said architecture of a parallel computer is constituted such that: a series of data having a stipulated relationship is given a space ID such that: a series of data having a stipulated relationship is given a space ID and the processor of each module manages a table that contains at least said space ID, the logical address of the portion of the series of data that it manages itself, the size of said portion and the size of the series of data,[See column 3, line 4-column 4, line1 and figure 8, where the MD Decoder and Address Generator of figure 5 that is within each memory module is illustrated. It is shown that data (having a relationship of being used by the processor) is uniquely labeled (a space ID) for identification and that the processor in each module detects the data and thus the ID is inherently stored so there is something to compare when detecting. It is also shown that an address of data is decoded and translated for access to main memory and thus stored for use. In addition figure 8 shows several registers (e.g., 140, 142, 112, 114, 118, 120, and 134) that store addresses of data of which the processor in the memory module manages. Also shown in that figure and in the text cited above, there are stored upper and lower limits of the addresses and thus a size of the data is known and stored. Since the processor manages all the data it uses, the portion of the series of data is in fact the entire series of data. Further all the collective storage

elements that store this data within the processor or memory module are viewed as a table.1]

iii. and the processor of each memory module determines if the portion of the series of data that is manages itself is involved in a received instruction, reads data stored in the RAM core and sends it out on a bus, writes data given via the bus to the RAM core, performs the necessary processing on the data , and/or updates said table. [The Examiner notes that the claim language of this limitation (specifically the placement of the and/or phrase: requires the reference need only show that portion of data managed by the processor performs any of the subsequent functions. As shown in the section cited above, the processor detects if the data is involved in a read or write and sending the data on the bus.]

b. Thiel does not explicitly disclose the memory modules having a RAM core, but only a local memory.

c. Hennessy has disclosed on pages 16 and 18 the use of RAM memory and that RAM (random access memory) differentiates from a sequential access memory in that memory access take the same amount of time no matter what portion of memory is read.

d. Hennessy has then shown on page 541 that RAM (SRAM and DRAM) have a much faster typical access time than a sequential memory such as a magnetic disk. This quick access time would have motivated one of ordinary skill in the art at the time of invention to modify the design

of Thiel to use a RAM as the local memory core rather than a sequential access memory.

18. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Thiel to use RAM as the local memory core rather than a sequential access memory so that typical memory accesses faster.

19. In regard to claim 10, Thiel in view of Hennessy discloses the information processing according to claim 9, wherein said CPU module is constituted such that it can be linked to another bus that connects legacy memory, input devices and display devices to each other [As shown above the CPU module controls all system function and thus if the devices of the claim are connected the module will control these devices as well. Examiner notes that the word "can" broadens the scope of the claim so that such a connection is not required, but only capable of performing such a function.]

20. In regard to claim 11, Thiel in view of Hennessy discloses a computer system comprising the information processing unit according to claim 9 and one or more storage devices including legacy memory , input deices and display devices linked to the CPU module via another bus [Column 11, lines 30-36 shows that the system performs image processing and computer graphics processing and thus connected to a display of sorts on another bus.]

21. In regard to claim 12 Thiel in view of Hennessy discloses the computer having architecture of a parallel computer of claim 1 and wherein the plurality of sets of buses are connected in parallel to the CPU module and to each memory module [In figure 5 of Thiel show buses oriented in parallel that are each has a

connection to processors and memory or input or output this is the same manner that each bus is shown in figure 1 in the instant application] although collectively the disclosed and claimed invention shows more buses due the inability of the claimed invention to simultaneously transmit data without arbitration then clearly the operation of the Thiel teachings is the same.] Note the CPU module provides a control signal on line 25 in the figure 1 to each memory module. Clearly this provides the arbitration so that only one memory module will transmit at time to/from the CPU and/or on any set of buses. Consequently the connection in the instant application is a shared one and that is the manner the claim is viewed.

22. In regard to claim 13, Thiel in view of Hennessy discloses a computer system comprising the information processing unit according to claim 9 and wherein the plurality of sets of buses are connected in parallel to the CPU module and to each memory module [In figure 5 of Thiel show buses oriented in parallel that are each has a connection to processors and memory or input or output this is the same manner that each bus is show in figure 1 in the instant application] although collectively the disclosed and claims invention shows more buses due the in ability of the claimed invention to simultaneously transmit data without arbitration then clearly the operation of the Thiel teachings is the same.] Note for the figures of the instant application the CPU module provides a control signal on line 25 in the figure 1 to each memory module. Clearly this provides the arbitration so that only one memory module will transmit at time to/from the CPU and/or on any set of buses. Consequently the connection in the instant application is a shared one and that is the manner the claim is viewed.

Response to Arguments

23. Applicant's arguments filed 5/12/05 have been fully considered but they are not persuasive.

24. In the remarks the Applicant argued in substance that

The Thiel reference does not teach an architecture of a parallel computer the Examiner contends as discussed in the outstanding rejection that system comprises plural computers that are for processing data and instruction and they each has processing means for processing at the same time the other processor processes instructions and data and therefore at least for these and the reasons stated in the outstanding rejection constitute an architecture of a parallel computer even though a parallel computer comprises the ability to perform multidimensional address it does not prevent it from processing data and instructions in parallel using the separate processors in the system As to the other limitation in the see the outstanding rejection above;

Applicant argues that Thiel does not teach each memory module contains a at least the space ID, the logical address of a portion of the series of data manged , the size of the portion and the size of the series of data The Examiner contends that Thiel taught this limitation as discussed in the outstanding rejection above.

Applicant agues Thiel does not teach the limitation of new claims 12 and 13. The Examiner contends that Theil taught the limitations to the extent claimed which is with respect the operation of the disclosed and claimed invention as discussed outstanding rejection above.

Applicant argues that Thiel does not teach a plurality of sets of busses

The Examiner contends However in addition to the discusion in the rejection above since in operation the buses must individually transfer data as indicated by a control signal from the CPU via a particular set of buses where the buses do not operate independent of the CPU in the claims of the instant application The plurality of sets of buses merely provide more lines for tranmission of data as was well known in the art for broadcasting data to plural elements of a information processing system such as memory.

As to the synchronization signal of claim 3, this is discussed the discussion of claim 3 in the outstanding rejection above.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will

the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER